

Docket No.: 043876-0147 PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of

Customer Number: 20277

Craig HANSEN, et al.

Confirmation Number: 6579

Application No.: 10/705,946

Group Art Unit: 2183

Filed: November 13, 2003

Examiner: Unknown

For: PROGRAMMABLE PROCESSOR AND METHOD FOR PARTITIONED GROUP SHIFT

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

Mail Stop Amendment Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313-1450

Dear Sir:

In accordance with the provisions of 37 C.F.R. 1.56, 1.97 and 1.98, the attention of the Patent and Trademark Office is hereby directed to the documents listed on the attached form PTO-1449. It is respectfully requested that the documents be expressly considered during the prosecution of this application, and that the documents be made of record therein and appear among the "References Cited" on any patent to issue therefrom.

Applicants are submitting to the Office a single paper copy of each of the documents listed on the attached form PTO-1449 in connection with a corresponding Supplemental Information Disclosure Statement filing for U.S. Patent Application No. 10/418,113. Applicants are separately filing a Petition requesting waiver of Rules 1.4(b) and 98(a)(2), which requires copies of the documents listed on the attached form PTO-1449 to be provided herewith. In view of the Office's practice of scanning documents into the Image File Wrapper, it is believed that providing a single set of paper copies will enable the Office to process the papers efficiently and expedite the

10/705,946

Examiner's consideration of the same. Furthermore, the attached form PTO-1449 includes citations to some materials for which it is difficult to obtain additional copies. In view of the Petition and in the interests of efficiency, Applicants' respectfully request that a copy of each of the cited documents be made of record in the present application.

This Information Disclosure Statement is being filed within three months of the U.S. filing date OR before the mailing date of a first Office Action on the merits. No certification or fee is required.

Applicants bring to the Examiner's attention the following pending applications of Craig C.

Hansen et al., which may include subject matter related to the present application:

Application Number	Title
10/418,113	Multiplier Array Processing System With Enhanced Utilization At Lower Precision
10/436,340	System With Wide Operand Architecture, And Method
10/616,303	Programmable Processor And Method With Wide Operations
10/646,787	Method And Software For Partitioned Group Element Selection Operation
10/712,430	System And Software For Catenated Group Shift Instruction
10/716,561	Programmable Processor And Method For Matched Aligned And Unaligned Storage Instructions
10/716,568	System And Software For Matched Aligned And Unaligned Storage Instructions
10/757,515	Method And Software For Multithreaded Processor With Partitioned Operations
10/757,516	Programmable Processor And System For Store Multiplex Operation
10/757,524	Programmable Processor And For Partitioned Group Element Selection Operation
10/757,836	Programmable Processor And System For Partitioned Floating-Point Multiply-Add Operation.

10/757,851	Method And Software For Partitioned Floating-Point Multiply-Add Operations
10/757,866	Method And Software For Store Multiplex Operation
10/757,925	Method And Software For Partitioned Group Element Selection Operation
10/757,939	Multithreaded Programmable Processor And System With Partitioned Operations

The attached form PTO-1449 includes (but is not exclusively limited to) documents that were cited in on-going litigation proceedings between the assignee of the present application, Dell Inc. and Intel Corp. (U.S. District Court for the Eastern District of Texas, Marshall Division (Civil Action No. 2:04-CV-120(TJW)). This litigation involves seven patents that are in the same family as each of the above applications.

Additionally, some documents were cited in related foreign applications. A copy of the foreign search report or office action is attached for the Examiner's information.

Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

McDERMOTT WILL & EMERY LLP

Richard E. Brown

Registration No. 47,453

600 13th Street, N.W. Washington, DC 20005-3096 Phone: 202.756.8000 REB:llg

Facsimile: 202.756.8087

Date: June 10, 2005

Please recognize our Customer No. 20277 as our correspondence address.

SHEET 1 OF 11

Pages, Columns, Lines, Where

Relevant Passages or Relevant

Figures Appear

INFORMATION DISCLOSURE CITATION IN AN APPLICATION

ATTY. DOCKET NO. **043876-0147**

SERIAL NO. **10/705,946**

APPLICANT

HANSEN, C., et al.

(PTO-1449)

US

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Document Number

Number-Kind Code2 (If known)

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Name of Patentee or Applicant of Cited

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Gafken

Brechard et al.

Lahti

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SERIAL NO. INFORMATION DISCLOSURE ATTY, DOCKET NO. 043876-0147 10/705.946 CITATION IN AN APPLICATION APPLICANT HANSEN, C., et al. FILING DATE **GROUP** (PTO-1449) 2183 **November 13, 2003** OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.) Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, **EXAMINER'S** INITIALS journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where CITE published. NO. L-1 Ide, et al., "A 320-MFLOPS CMOS Floating-point Processing Unit for Superscalar Processors," p. 12-21, 28 March 1993, IEEE J. OF SOLID-STATE CIRCUITS. K. Uchiyama et al., The Gmicro/500 Superscalar Microprocessor with. Branch Buffers, IEEE L-2 Micro, October 1993, p. 12-21. L-3 Ruby B. Lee, Realtime MPEG Video Via Software Decompression on a PA-RISC Processor, IEEE (1995). L-4 Karl M. Guttag et al. "The TMS34010: An Embedded Microprocessor", IEEE June 1988, p. 186-190. L-5 M. Awaga et al., "The µVP 64-bit Vector Coprocessor: A New Implementation of High-Performance Numerical Computation", IEEE Micro, Vol. 13, No. 5, October 1993, p.24-36. L-6 Tom Asprey et al., "Performance Features of the PA7100 Microprocessor", IEEE Micro (June 1993), p. 22-35. Gove, Robert J., "The MVP: A Highly-Integrated Video Compression Chip," IEEE Data Compression Conf., March (1994), pp. 215-224. L-8 Woobin Lee, et al., "Mediastation 5000: Integrating Video and Audio," IEEE Multimedia, 1994, pp. 50-61. L-9 Karl, Guttag et. al "A Single-Chip Multiprocessor for Multimedia: The MVP," IEEE Computer Graphics & Applications, November, 1992, p. 53-64. TMS32OC8O (MVP) Master Processor User's Guide, Texas Instruments, March, 1995, p. 1-33. L-11 TMS320C80 (MVP) Parallel Processor User's Guide ["PP"]; Texas Instruments March 1995, p. L-12 Shipnes, Julie, "Graphics Processing with the 88110 RISC Microprocessor," IEEE COMPCOM, (Spring, 1992) pp. 169-174. L-13 ILLIAC IV: Systems Characteristics and Programming Manual, May 1, 1972, p. 1-78. L-14 N. Abel et al., ILLIAC IV Doc. No. 233, "Language Specifications for a Fortran-Like Higher Level Language for ILLIAV IV, August 28, 1970, p. 1-51. ILLIAC IV Quarterly Progress Report: October, November, December 1969; Published January 15, 1970, pp. 1-15. L-16 N.E. Abel et al., Extensions to Fortran for Array Processing (1970) pp. 1-16. DATE CONSIDERED **EXAMINER**

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INFORMATION DISCLOSURE SERIAL NO. ATTY. DOCKET NO. 043876-0147 10/705,946 CITATION IN AN APPLICATION APPLICANT HANSEN, C., et al. FILING DATE **GROUP** (PTO-1449) November 13, 2003 2183 OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.) Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, **EXAMINER'S** INITIALS journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where CITE NO. L-87 Hwang & Degroot, "Parallel Processing for Supercomputers & Artificial Intelligence," 1993. L-88 Nienhaus, Harry A., "A Fast Square Rooter Combining Algorithmic and Table Lookup Techniques," IEEE Proceedings Southeastcon, 1989 pp 1103-1105. L-89 Eisig, David, et al., "The Design of a 64-Bit Integer Multiplier/Divider Unit," IEEE 1993 pp 171-178. L-90 Margulis, Neal, "i860 Microprocessor Architecture," Intel Corporation 1990. L-91 Intel Corporation, 3860 XP Microprocessor Data Book" (May 1991). L-92 Hewlett-Packard, "HP 9000 Series 700 Workstations Technical Reference Manual Model 712 (System)" January 1 994. L-93 Ruby Lee, et al., Pathlength Reduction Features in the PA-RISC Architecture Feb. 24-28, 1992 p. 129-135. Kevin Wadleigh et al., High Performance FFT Algorithms for the Convex C4/XA Supercomputer, Poster, Conference on Supercomputing, Washington, D.C., Nov. 1994. L-95 Fields, Scott, "Hunting for Wasted Computing Power: New Software for Computing Networks Puts Idle PC's to Work," Univ. of Wisconsin- Madison 1993 p. 1-8. L-96 Litzkow et al., "Condor - A Hunter of Idle Workstations," IEEE (1988) p. 104-111. L-97 Gregory Wilson, The History of the Development of Parallel Computing" http://ei.cs.vt.edu/history/Parallel.html, p. 1-38. Marsha Jovanovic and Kimberly Claffy, Computational Science: Advances Through Collaboration" "Network Behavior" San Diego Supercomputer Center 1993 Science Report, p. 1-11 [http://www.sdsc.edu/Publications/SR93/network behavior.html]. L-99 National Science Foundation (NSF) [www.itrd.gov/pubs/blue94/section.4.2.html] 1994. L-100 Intel Corporation, "Paragon User's Guide" (Oct. 1993). L-101 Turcotte, Louis H., "A Survey of Software Environments for Exploiting Networked Computing Resources" Engineering Research Center for Computational Field Simulation June 11, 1993, p. 1-150. **EXAMINER** DATE CONSIDERED

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